# FPGA/SoC based GigE Vision Stack

## DIPC-7050 - Datasheet

## HIGHLIGHTS

- GigE Vision standard compliant (version 2.1)
- 1/10 Gigabit Ethernet support
- Low and deterministic latency
- Modular, scalable and easy to use
- Enables high-performance image processing

## OVERVIEW

The DIPC-7050 GigE Vision Stack is a system architecture for operating GigE Vision standard compliant cameras in a FPGA/SoC- based environment. It provides several functionalities in firmware and software for operating devices in a modular and customizable way, and it is usable in wide array of applications.

One of the main advantages is having cameras image data stream directly in programmable logic using the AXI4-Stream Video protocol. In this way users are able to run their own high performance image processing operations immediately in hardware with multiple instances in parallel.

DIPC-7050 comes with two IP modules for running GigE Vision Standard related functions as well as up to 10 Gigabit Ethernet interfacing between programmable logic and connected devices. These cores are implemented with further infrastructure functionality blocks related to Xilinx Vivado Design Suite.

Appropriate controller software for on-chip register configuration runs as a command server. Applications on software side are optional. If used they can be connected to command server via a TCP/IP socket.

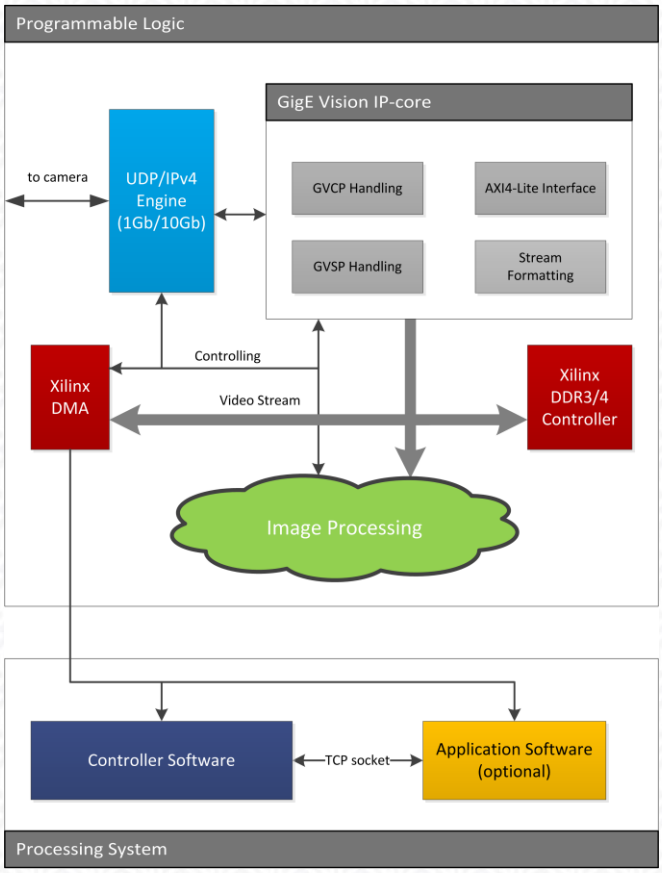


Figure 1: DIPC-7050 System Architecture

## FEATURES

- Support for Xilinx 7-series, Zynq, UltraScale and UltraScale+ devices
- AXI4 compliant interfaces
- Synchronization between camera devices using IEEE1588 or external trigger
- Support for x86 and ARM architectures
- Reference implementation for Xilinx Evaluation (KCU116) board is available
- Separate documentation for Users and Developers available

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## SYSTEM REQUIREMENTS

For using DIPC-7050 in a single channel configuration, the following components are needed:

- Xilinx FPGA/SoC platform (7-series, Zynq, Ultrascale, Ultrascale+, MPSoC)
- 125MHz/312.5MHz Ethernet ref. Clock
- CPU to AXI access (PCIe endpoint or PS master)
- CPU for running Controller Software (Linux, SoC PS or external)
- Optical or copper (RJ45) SFP+ connector to PL transceiver or external PHY (e.g. RJ45)
- DDR3/DDR4 on-board memory (preferably)

## ARCHITECTRUAL CONCEPT

The DIPC-7050 consists of a programmable logic firmware and a processing system software part. The firmware, especially the UDP IP-core and the GigE Vision IP-core, realizes camera communication and image stream handling. Behind GigE Vision IP-core image stream is split into two in the example design. One gets stored into on-board memory the other is feed into the real-time image processing module. Results can be either read out by software or can be stored in memory. The FPGA/SoC programmable logic is connected via Direct Memory Access to the Controller Software running on the CPU and supervising the entire system.

From a user perspective, it is only necessary to start the Controller Software command server, establish a connection and send suitable commands, either from a Telnet session or using an Application Software example. Both are connected via TCP/IP socket.

## REFERENCE IMPLEMENTATION

For getting access to DIPC-7050 functionalities, a reference implementation for the Xilinx KCU116 evaluation board is available. Using the Quick Start Guide, users are able to get results from a single channel image processing system within 30 minutes. The following table gives an overvwie about the DIPC-7050 programmable logic resource consumption on the Xilinx KCU116 evaluation board (xcku5p-ffvb676-2-e):

| MODULES | DESCRIPTION | RESOURCES | |
|---|---|---|---|
| GigE Vision IP-core | Implementation of GigE Vision standard related functionalities for camera communication, configuration and image video stream parsing. Data output uses AXI4-Stream Video Protocol. | Registers | 1303 |
| | | Lookup Tables | 2103 |
| | | BlockRAMs | 10 |
| UDP IP-core | UDP/IPv4 core for data packaging and parsing between UDP/IPv4 packets and AXI4-Stream for on chip communication. The core also contains ARP and ICMP functionalities to ping the core. | Registers | 2295 |
| | | Lookup Tables | 2362 |
| | | BlockRAMs | 12 |
| Image Processing (Demo) | Demo image processing IP-core for calculating 2-dimensional Standard Deviation and Mean of incoming video stream. The module is implemented in Xilinx Vivado HLS. | Registers | 1572 |
| | | Lookup Tables | 1529 |
| | | DSP | 25 |
| | | BlockRAMs | 9 |
| Toplevel | DIPC-7050 toplevel design with whole functionality including infrastructure like AXI interconnect, clock generation, transceivers, memory interface (Xilinx DDR4 MIG) and PCIe. | Registers | 70507 (16%) |
| | | Lookup Tables | 59948 (25%) |
| | | DSP | 28 (2%) |
| | | BlockRAMs | 127 (25%) |



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